**SOLUTION**

CSC332 Spring 2021 HW2 (Ch 3. Interrupts)

**Due: Thurs March 22 11:59 PM**

**Submit your solution on Blackboard (BB), not my email.**

**Please write your answers in WORD, Wordpad, Notepad, or pdf files and upload it to the system.**

**Do only one question, based on the first letter of your last name:**

**A-M: Q1**

**N-Z: Q2**

Q1.

Consider the interrupt mechanism discussed in class with the following modification. On occurrence of the interrupt, the hardware will load only the new PC value (from the interrupt vector), and not the PSW value.

A special machine instruction is provided, which would load the new PSW value (corresponding to the most recent interrupt that has occurred) from the interrupt vector.

Assume that the logical and physical addresses are same.

There are no other changes to the interrupt mechanism

that we discussed in class.

What could go wrong with this scheme?

Explain in LESS THAN 50 WORDS.

**Answer:**

Consider the instruction to load new PSW from Interr Vector.

Is this instruction privileged or non-privileged?

If priv, then service routine cannot execute it since mode=user.

If non-priv, then any user can execute it to get new PSW value from Interr Vector and it would be in sup mode.

Q2.

At the end of a service routine, suppose we have two RTI instructions one after other. Will something go wrong? Explain.

Ans. Nothing will go wrong. Second RTI will not be executed.